What is claimed is:

1. A method of controlling a multiple-level inverter bridge with a two-level induction motor controller, the two-level induction motor controller outputting six modulated signals for controlling switching of six switches in a two-level inverter bridge, said method comprising:

converting the six modulated signals into N time-coordinated signals, wherein $N \geq 12$ and N is an integer-multiple of 3;

controlling N switches of the multiple-level inverter bridge by applying the N time-coordinated signals,

wherein the multiple-level inverter bridge comprises three branches, each branch having N/3 switches and producing one phase of a three-phase output of the multiple-level inverter bridge, and never-less-than N/6 of the N/3 switches of a respective branch of the multiple level inverter bridge having a logical-off state.

2. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 1,

wherein the six modulated signals are further characterized as being three pairs of modulated signals A_{1b} and A_{2b} ($b \in \{1, 2, 3\}$), each pair of modulated signals intended for controlling one-of-three branches of a two-level inverter bridge, each branch b producing one phase of a three-phase output of a two-level inverter bridge;

said step of converting the six modulated signals into N time-coordinated including:

generating three sets of time-coordinated signals S_{1b} to $S_{(N/3)b}$ from the three pairs of modulated signals A_{1b} and A_{2b} output by the two-level induction motor controller, each

set of time-coordinated signals S_{1b} to $S_{(N/3)b}$ being timed to control the switches of branch b of the multiple-level inverter bridge, timing of each set of time-coordinated signals S_{1b} to $S_{(N/3)b}$ varying based on at least a delay time of the switches of the respective branch b, and for each branch b, never-less-than N/6 of the time-coordinated signals S_{1b} to $S_{(N/3)b}$ having a logical-off state; and

said step of controlling said N switches of the multiple-level inverter bridge including:

applying each set b of time-coordinated signals S_{1b} to $S_{(N/3)b}$ to the N/3 switches of a corresponding branch b of the multiple-level inverter bridge.

3. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 2, said step of generating three sets of time-coordinated signals S_{1b} to $S_{(N/3)b}$ from the three pairs of modulated signals A_{1b} and A_{2b} comprising:

for time-coordinated signals S_{1b} to $S_{(N/6)b}$, forming each S_{yb} to have a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

for time-coordinated signals $S_{(N/6+1)b}$ to $S_{(N/3)b}$, forming each S_{zb} to have a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

4. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 2, said step of generating the three sets of time-coordinated signals S_{1b} to $S_{(N/3)b}$ from the three pairs of modulated signals A_{1b} and A_{2b} comprising:

forming time-coordinated-signals S_{1b} to $S_{(N/6)b}$ by adding a turn-on delay $d_{1x}\cdot\Delta t_b$, and a turn-off delay $d_{2x}\cdot\Delta t_b$, to the modulated signal A_{1b}; and

forming time-coordinated signals $S_{(N/3)b}$ to $S_{(N/6+1)b}$ by adding a turn-on delay $d_{1x}\cdot\Delta t_b$,

and a turn-off delay $d_{2x} \cdot \Delta t_b$, to the modulated signal A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of N/3 switches in a branch b of the multiple-level inverter bridge, $d_{1x} \geq 0$, $d_{2x} \geq 0$, and $x = 1$ to N/6, and

wherein every d_{1x} has a different value, and every d_{2x} has a different value.

5. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 4,

wherein for time-coordinated signals S_{1b} to $S_{(N/6)b}$, each S_{yb} has a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

wherein for time-coordinated signals $S_{(N/6+1)b}$ to $S_{(N/3)b}$, each S_{zb} has a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

6. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 2,

wherein the multiple-level inverter has three levels and N = 12, each branch b of the three-level inverter comprising four switches connected in series and controlled by time-coordinated signals S_{1b}-S_{4b}; and

said step of generating the three sets of time-coordinated signals S_{1b}-S_{4b} from the three pair of modulated signals A_{1b} and A_{2b} comprising:

forming time-coordinated signal S_{1b} by adding a turn-on delay of $3\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{2b} by adding a turn-on delay of Δt_b and a turn-off delay of $2\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{3b} by adding a turn-on delay of Δt_b and a

turn-off delay of $2\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{4b} by adding a turn-on delay of $3\Delta t_b$ to the modulated signal A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of the four switches in the respective branch b.

7. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 2,

wherein the multiple-level inverter has four levels and N = 18, each branch b of the four-level inverter comprising six switches connected in series and controlled by time-coordinated signals S_{1b}-S_{6b}; and

said step of generating the three sets of time-coordinated signals S_{1b}-S_{6b} from the three pair of modulated signals A_{1b} and A_{2b} comprising:

forming time-coordinated signal S_{1b} by adding a turn-on delay of $5\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{2b} by adding a turn-on delay of $3\Delta t_b$ and a turn-off delay of $2\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{3b} by adding a turn-on delay of Δt_b and a turn-off delay of $4\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{4b} by adding a turn-on delay of Δt_b and a turn-off delay of $4\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{5b} by adding a turn-on delay of $3\Delta t_b$ and a turn-off delay of $2\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{6b} by adding a turn-on delay of $5\Delta t_b$ to the

modulated signal A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of the six switches in the respective branch b.

8. The method of controlling a multiple-level inverter bridge with a two-level induction motor controller as defined in claim 2,

wherein the multiple-level inverter has five levels and $N = 24$, each branch b of the five-level inverter comprising eight switches connected in series and controlled by time-coordinated signals S_{1b}-S_{8b}; and

said step of generating the three sets of time-coordinated signals S_{1b}-S_{8b} from the three pair of modulated signals A_{1b} and A_{2b} comprising:

forming time-coordinated signal S_{1b} by adding a turn-on delay of $7\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{2b} by adding a turn-on delay of $5\Delta t_b$ and a turn-off delay of $2\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{3b} by adding a turn-on delay of $3\Delta t_b$ and a turn-off delay of $4\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{4b} by adding a turn-on delay of Δt_b and a turn-off delay of $6\Delta t_b$ to the modulated signal A_{1b};

forming time-coordinated signal S_{5b} by adding a turn-on delay of Δt_b and a turn-off delay of $6\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{6b} by adding a turn-on delay of $3\Delta t_b$ and a turn-off delay of $4\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{7b} by adding a turn-on delay of $5\Delta t_b$ and a

turn-off delay of $2\Delta t_b$ to the modulated signal A_{2b};

forming time-coordinated signal S_{8b} by adding a turn-on delay of $7\Delta t_b$ to the modulated signal A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of the eight switches in the respective branch b.

9. An adapter circuit for controlling a multiple-level inverter bridge with a two-level induction motor controller, the two-level induction motor controller outputting six modulated signals for controlling switching in a two-level inverter bridge, and the multiple-level inverter bridge having $N \geq 12$ switches divided into 3 branches, the adapter circuit, comprising:

three pairs of modulated signal inputs A_{1b} and A_{2b} ($b \in \{1, 2, 3\}$), whereby the six modulated signals from the two-level induction motor controller are input;

three sets of time-coordinated signal outputs S_{1b} to $S_{(N/3)b}$, wherein each set b of time-coordinated signals output via S_{1b} to $S_{(N/3)b}$ is timed to control N/3 switches of branch b of the multiple-level inverter bridge; and

timing circuitry comprising circuitry selected from the group consisting of combinatorial circuits, sequential circuits, delay elements, analog-based logic gates, programmable logic, and a combination thereof, generating time-coordinated signals output via S_{1b} to $S_{(N/6)b}$ from modulated signals input via A_{1b}, and generating time-coordinated signals output via $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from modulated signals input via A_{2b}, adding at least a turn-on delay or turn-off delay to each modulated signal input via A_{1b} and A_{2b},

wherein for each set b of time-coordinated signals output via S_{1b} to $S_{(N/3)b}$, never-less-than N/6 of the N/3 time-coordinated signals has a logical-off state.

10. The adapter circuit as defined in claim 9,

wherein for time-coordinated signals output via S_{1b} to $S_{(N/6)b}$, each S_{yb} has a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

wherein for time-coordinated signals output via $S_{(N/6+1)b}$ to $S_{(N/3)b}$, each S_{zb} has a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

11. The adapter circuit as defined in claim 9,

wherein within each set b of time-coordinated signals output via S_{1b} to $S_{(N/3)b}$:

each time-coordinated signal output via S_{1b} to $S_{(N/6)b}$ is formed by adding a turn-on delay $d_{1x}\cdot\Delta t_b$ and a turn-off delay $d_{2x}\cdot\Delta t_b$ to the modulated signal input via A_{1b}; and

each time-coordinated signal output via $S_{(N/3)b}$ to $S_{(N/6+1)b}$ is formed by adding a turn-on delay $d_{1x}\cdot\Delta t_b$ and a turn-off delay $d_{2x}\cdot\Delta t_b$, to the modulated signal input via A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of N/3 switches in a branch b of the multiple-level inverter bridge, $d_{1x} \geq 0$, $d_{2x} \geq 0$, and x = 1 to N/6, and

wherein every d_{1x} has a different value, and every d_{2x} has a different value.

12. The adapter circuit as defined in claim 11,

wherein for time-coordinated signals output via S_{1b} to $S_{(N/6)b}$, each S_{yb} has a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

wherein for time-coordinated signals output via $S_{(N/6+1)b}$ to $S_{(N/3)b}$, each S_{zb} has a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

13. The adapter circuit as defined in claim 11, wherein $N = 12$, $d_{11} = 3$, $d_{12} = 1$, $d_{21} = 0$, and $d_{22} = 2$.

14. The adapter circuit as defined in claim 11, wherein $N = 18$, $d_{11} = 5$, $d_{12} = 3$, $d_{13} = 1$, $d_{21} = 0$, $d_{22} = 2$, and $d_{23} = 4$.

15. The adapter circuit as defined in claim 11, wherein $N = 24$, $d_{11} = 7$, $d_{12} = 5$, $d_{13} = 3$, $d_{14} = 1$, $d_{21} = 0$, $d_{22} = 2$, $d_{23} = 4$, and $d_{24} = 6$.

16. The adapter circuit as defined in claim 9, said combinatorial circuits comprising AND and OR gates, and said sequential circuits comprising flip-flops.

17. The adapter circuit as defined in claim 9, wherein said adapter circuit comprises a Complex Programmable Logic Device.

18. An adapter for controlling a multiple-level inverter bridge with a two-level induction motor controller, the two-level induction motor controller outputting six modulated signals for controlling switching in a two-level inverter bridge, and the multiple-level inverter bridge having $N \geq 12$ switches divided into 3 branches, the adapter, comprising:

three pairs of modulated signal inputs A_{1b} and A_{2b} ($b \in \{1, 2, 3\}$), whereby the six modulated signals from the two-level induction motor controller are input;

three sets of time-coordinated signal outputs S_{1b} to $S_{(N/3)b}$, wherein each set b of time-

coordinated signals output via S_{1b} to $S_{(N/3)b}$ is timed to control N/3 switches of branch b of the multiple-level inverter bridge; and

first conversion means for generating time-coordinated signals output via S_{1b} to $S_{(N/6)b}$ from a modulated signals input via A_{1b}, adding at least a turn-on delay or turn-off delay to generate S_{1b} to $S_{(N/6)b}$ from the modulated signal input via A_{1b},

second conversion means for generating time-coordinated signals output via $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from a modulated signal input via A_{2b}, adding at least a turn-on delay or turn-off delay to generate $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from the modulated signal input via A_{2b},

wherein for each set b of time-coordinated signals output via S_{1b} to $S_{(N/3)b}$, never-less-than N/6. of the N/3 time-coordinated signals has a logical-off state.

19. An induction motor drive system for driving a three-phase motor, comprising:

a two-level induction motor controller, outputting signals for controlling a two-level inverter bridge;

a multiple-level inverter bridge, having $N \geq 12$ switches arranged to form 3 branches, each branch providing one phase of a three-phase output for driving the three-phase motor; and

an adapter circuit, generating N time-coordinated signals controlling the N switches of the multiple-level inverter bridge from said signals output by the two-level induction motor controller.

20. The induction motor drive system as defined in claim 19,

wherein the signals output from the two-level induction motor controller comprise three pairs of modulated signal inputs A_{1b} and A_{2b} ($b \in \{1, 2, 3\}$), intended for controlling switching in a two-level inverter bridge; and

wherein the N-time coordinated signals are further characterized as being three sets of time-coordinated signals S_{1b} to $S_{(N/3)b}$, each set being timed to control the N/3 switches of branch b of the multiple-level inverter bridge, and within each set b, never-less-than N/6 of the time-coordinated signals S_{1b} to $S_{(N/3)b}$ having a logical-off state; and

wherein the adapter circuit comprises circuits selected from the group consisting of combinatorial circuits, sequential circuits, delay elements, analog-based logic gates, programmable logic, and a combination thereof generating the time-coordinated signals S_{1b} to $S_{(N/6)b}$ from the modulated signal A_{1b}, and timing circuitry generating time-coordinated signals $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from the modulated signal A_{2b}, forming S_{1b} to $S_{(N/3)b}$ by adding at least a turn-on delay or turn-off delay to the modulated signal A_{1b} and A_{2b}.

21. The induction motor drive system as defined in claim 20,

wherein for time-coordinated signals S_{1b} to $S_{(N/6)b}$, each S_{yb} has a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

wherein for time-coordinated signals $S_{(N/6+1)b}$ to $S_{(N/3)b}$, each S_{zb} has a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

22. The induction motor drive system as defined in claim 20,

wherein within each set b of time-coordinated signals S_{1b} to $S_{(N/3)b}$:

each time-coordinated signal S_{1b} to $S_{(N/6)b}$ is formed by adding a turn-on delay $d_{1x}\cdot\Delta t_b$ and a turn-off delay $d_{2x}\cdot\Delta t_b$ to the modulated signal A_{1b}; and

each time-coordinated signal $S_{(N/3)b}$ to $S_{(N/6+1)b}$ is formed by adding a turn-on delay $d_{1x}\cdot\Delta t_b$ and a turn-off delay $d_{2x}\cdot\Delta t_b$, to the modulated signal A_{2b};

wherein Δt_b is a turn-off delay time of a switch with a longest turn-off delay time of

N/3 switches in a branch b of the multiple-level inverter bridge, $d_{1x} \geq 0$, $d_{2x} \geq 0$, and x = 1 to N/6, and

wherein every d_{1x} has a different value, and every d_{2x} has a different value.

23. The induction motor drive system as defined in claim 22,

wherein for time-coordinated signals S_{1b} to $S_{(N/6)b}$, each S_{yb} has a logical-on state after, and a logical-off state before, $S_{(y+1)b}$, y being a series of integers from 1 to (N/6-1), and

wherein for time-coordinated signals $S_{(N/6+1)b}$ to $S_{(N/3)b}$, each S_{zb} has a logical-on state after, and a logical-off state before, $S_{(z-1)b}$, z being a series of integers from (N/6+2) to (N/3).

24. The induction motor drive system as defined in claim 19,

wherein the signals output from the two-level induction motor controller comprise three pairs of modulated signal inputs A_{1b} and A_{2b} ($b \in \{1, 2, 3\}$), intended for controlling switching in a two-level inverter bridge; and

wherein the N-time coordinated signals are further characterized as being three sets of time-coordinated signals S_{1b} to $S_{(N/3)b}$, each set being timed to control the N/3 switches of branch b of the multiple-level inverter bridge, and within each set b, never-less-than N/6 of the time-coordinated signals S_{1b} to $S_{(N/3)b}$ having a logical-off state; and

wherein the adapter circuit comprises:

first conversion means for generating time-coordinated signals output via S_{1b} to $S_{(N/6)b}$ from a modulated signals input via A_{1b}, adding at least a turn-on delay or turn-off delay to generate S_{1b} to $S_{(N/6)b}$ from the modulated signal input via A_{1b}, and

second conversion means for generating time-coordinated signals output via $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from a modulated signal input via A_{2b}, adding at least a turn-on delay or turn-off delay to generate $S_{(N/6+1)b}$ to $S_{(N/3)b}$ from the modulated signal input via A_{2b}.

25. A method of controlling a multiple-level inverter bridge with a two-level induction motor controller, the two-level induction motor controller comprising a regulator and an internal modulator for a two-level inverter bridge, command signals being output from the regulator for control of the internal modulator, the method comprising:

outputting the command signals from the two-level induction motor controller via a first interface port of the two-level induction motor controller;

transmitting the command signals output from said first interface port via a serial or parallel connection;

inputting the transmitted command signals into an external adapter circuit via a second interface port, said adapter circuit comprising a modulator; and

generating, in the modulator of the external adapter circuit and based on the command signals input via said second interface port, twelve-or-more time-coordinated signals for controlling an inverter bridge having three-or-more levels.

26. The method of controlling a multiple-level inverter bridge as defined in claim 25, further comprising:

controlling twelve-or-more switches in a multiple-level inverter bridge by applying the twelve-or-more time-coordinated signals generated by the modulator of the external adapter circuit.

27. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein said steps of outputting, transmitting, and inputting result in updated command signals being periodically provided to the external adapter circuit.

28. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the two-level induction motor controller utilizes vector control, said regulator being a flux and torque regulator and said command signals output from the two-level induction motor controller being flux (d) and torque (q) command signals.

29. The method of controlling a multiple-level inverter bridge as defined in claim 28, said method further comprising:

transforming the flux (d) and torque (q) command signals into α and β command signals via a Park Transform, after inputting the transmitted command signals into the external adapter circuit, but before generating the twelve-or-more time coordinated signals in the modulator, said modulator of the external adapter circuit generating the twelve-or-more time coordinated signals using the α and β command signals.

30. The method of controlling a multiple-level inverter bridge as defined in claim 28, said method further comprising:

transforming the flux (d) and torque (q)command signals into signals α and β signals via a Park Transform, after inputting the transmitted command signals into the external adapter circuit,

transforming signals α and β into three-phase a, b, and c command signals, before generating the twelve-or-more time coordinated signals in the modulator, said modulator of the external adapter circuit generating the twelve-or-more time coordinated signals using the a, b, and c command signals.

31. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the two-level induction motor controller utilizes vector control, said regulator being a flux and torque regulator and said command signals output from the two-level induction motor controller being α and β command signals.

32. The method of controlling a multiple-level inverter bridge as defined in claim 31, said method further comprising:

transforming the α and β command signals into three-phase a, b, and c command signals, after inputting the transmitted command signals into the external adapter circuit, but before generating the twelve-or-more time coordinated signals in the modulator, said modulator of the external adapter circuit generating the twelve-or-more time coordinated signals using the a, b, and c command signals.

33. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the two-level induction motor controller utilizes vector control, said regulator being a flux and torque regulator and said command signals output from said two-level induction motor controller being three-phase a, b, and c command signals.

34. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the two-level induction motor controller utilizes scalar control, said regulator being a voltage regulator and said command signals output from said two-level induction motor controller being frequency and voltage command signals.

35. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the first interface port is a Controller Area Network serial interface.

36. The method of controlling a multiple-level inverter bridge as defined in claim 25, wherein the modulator of the external adapter circuit is selected from the group consisting of a space-vector modulator, a hysteresis modulator, pulse pattern modulator, and a sine-triangle modulator.